REMARKS

Claims 1-23 are pending. By this Amendment claims 1, 7, 9 and 14-23 are amended. Reconsideration in view of the above amendments and following remarks is respectfully requested.

Claims 7, 19 and 21 were objected to. Claims 7, 19 and 21 have been amended in accordance with the suggestion of the Office Action. Reconsideration and withdrawal of the objection are respectfully requested.

Claims 1, 2, 4-9 and 11-13 were rejected under 35 U.S.C. § 102(e) over Patel (U.S. Patent 6,839,258). The rejection is respectfully traversed.

The instant application is the national phase of International (PCT) Application PCT/KR03/00051, filed January 10, 2003. That application was filed in English and designated the United States. (See WO 03/058635 A1, the publication of PCT/KR03/00051, published July 17, 2003, in English.) Accordingly, the instant application has an effective U.S. filing date of January 10, 2003. See 35 U.S.C. § 365(c).

In addition, PCT/KR03/00051 claimed priority to U.S. Application 60/346,897, filed January 11, 2002. Accordingly, the instant application has an effective U.S. filing date of January 11, 2002 for all claimed subject matter disclosed in U.S. Application 60/346,897.

Patel has a U.S. filing date of May 12, 2003, which is after both January 10, 2003 and January 11, 2002. Accordingly, Patel was not filed by another in the United States prior to Applicant. Therefore, Patel is not prior art under 35 U.S.C. § 102(e)(2).

Reconsideration and withdrawal of the rejection over Patel are respectfully requested.

Claims 14-16 were rejected under 35 U.S.C. § 102(b) over Tanaka et al. (U.S. Patent 5,559,737). The rejection is respectfully traversed.

Claim 14 recites a semiconductor memory device comprising a precharging circuit configured and arranged to precharge a bitline and a reference bitline; a memory cell configured and arranged to share charge with the bitline; a bias circuit configured and arranged to bias a potential of the reference bitline to increase a refresh period in a semiconductor memory device; and a sense amplifier configured and arranged to sense a difference between a potential of the bitline and a potential of the reference bitline.

Tanaka et al. do not disclose or suggest a bias circuit configured and arranged to bias a potential of the reference bitline to increase a refresh period in a semiconductor memory device, as recited in claim 14. Tanaka et al. disclose a bias circuit 6 that applies a predetermined bias potential (e.g. about 3 V) to the transistors 4 and 5 during read access, i.e.

so as to maintain a turn-on state during data access. See column 1, lines 46-48. The dummy bias circuit 16 operates in a similar manner to the bias circuit 6. See column 1, lines 53-57.

As Tanaka et al. do not disclose or suggest all the limitations of claim 14, Tanaka et al. cannot anticipate or render obvious claim 14.

Claims 15 and 16 recite additional features of the invention and are allowable for the same reasons discussed above with respect to claim 14 and for the additional features recited therein.

Reconsideration and withdrawal of the rejection over Tanaka et al. are respectfully requested.

In view of the above amendments and remarks, Applicants respectfully submit that all claims are allowable and that the entire application is in condition for allowance.

Should the Examiner believe that anything further is desirable to place the application in better condition for allowance, the Examiner is invited contact the undersigned at the telephone number listed below.

Respectfully submitted,
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